# Session 13 Overview

# ΔΣ ADCs and Converter Techniques

**Chair:** Zhongyuan Chang, *IDT-Newave Technology, Shanghai, China*

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The ever-increasing data rates in multi-standard wireless communication systems demands for wireless receivers with higher dynamic range and wider bandwidth. Further, the power consumption of the receiver building blocks should be kept at minimum. Reconfigurable ΔΣ modulators are the promising ADC topologies to cope with multi-standard challenges due to their power efficiency and high SNR. This session highlights the advances in ΔΣ modulators and other converter techniques that enhance the dynamic range and power consumption of ADCs.

In Paper 13.1 from NXP Semiconductors, a quadrature ΔΣ modulator with 77dB dynamic range and 20MHz bandwidth for near-zero-IF wideband receivers is presented. The quadradure modulator employs a cascade of 2 continuous-time modultors with a digital quadrature noise-cancellation filter. Implemented in 90nm CMOS, the modulator achieves 71dB SNR in 20MHz bandwidth.

In the next 3 papers, the authors report the implementation of ΔΣ modulators that are targeting multi-band wireless applications. Paper 13.2 from Advanced Circuit Pursuit and ETH describes a 0.13μm tri-mode (EDGE/UMTS/WLAN) ΔΣ ADC with -92dB THD. The modulator employs a 2-2 cascaded feedforward topology with reduced integrator swing for 1.2V operation. Low power and reconfigurability are achieved by programming optimal oversampling frequency and opamp biasing. In Paper 13.3 from NXP Semiconductors, the implementation of a reconfigurable continuous-time $5^{th}$-order single-bit ΔΣ modulator in 90nm CMOS is presented. The modulator consists of a continuous-time feedforward loop filter combined with switched-capacitor feedback DAC to minimize the effect of clock jitter. The extensive reconfigurability of 121 modes with dynamic-range/bandwidth of 85dB/100kHz to 52dB/10MHz is demonstrated covering the whole range of GSM to WLAN/WiMAX applications. The next paper, 13.4 from NXP Semiconductors, reports a $5^{th}$-order ΔΣ modulator embedded in an EDGE/CDMA/UMTS receiver in 65nm CMOS. By combining a front-end continuous-time integrator with discrete-time $2^{nd}$- to $5^{th}$-stage integrators, low power and accurate transfer function are achieved. An open-loop switched-capacitor OTA is used for the discrete-time integrator allowing fast settling with low power consumption resulting in an FOM as low as 0.25pJ/conversion-step.

Low-power and high-speed SAR converter techniques are demonstrated in the next 2 papers that push the performance limit of conventional SAR ADCs. A charge-sharing SAR ADC in Paper 13.5 from IMEC reports an FOM of 65fJ/conversion-step by using the passive charge-sharing techniques, dynamic offset calibration, and an asynchronous controller. Paper 13.6 from Infineon reports a 14b 2× time-interleaved SAR ADC operating at 480MHz with redundancy pushing the conversion rate up to 40MS/s with 66mW in 0.13μm CMOS, which surpasses previously achieved performance by pipelined ADCs.

The last paper, 13.7 from Infineon, reports a 13b 25mW 200MS/s DAC in 0.13μm CMOS operating at 1.5V. Two novel background calibration techniques are proposed: the nested background calibration trims all segments without the use of current splitters, and randomized period calibration converts spurious tones into wideband noise resulting in 87.3dB SFDR.

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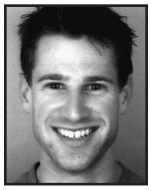
**13.1 A 56mW CT Quadrature Cascaded ΔΣ Modulator with 77dB DR in a Near Zero-IF 20MHz Band** **8:30 AM**

*L. Breems,* NXP Semiconductors Research, Eindhoven, The Netherlands

A 90nm CMOS CT quadrature ΔΣ modulator is designed for highly digitized wideband receivers. The ADC achieves 77dB DR and 20MHz BW around a 10.5MHz IF and is sampled at 340MHz. The cascaded modulator comprises programmable analog 2nd-order quadrature filters and a digital quadrature noise-cancellation filter. The 0.5mm² chip draws 56mW from a 1.2V supply.



**13.2 A 0.13µm CMOS EDGE/UMTS/WLAN Tri-Mode ΔΣ ADC with -92dB THD** **9:00 AM**

*T. Christen,* Advanced Circuit Pursuit, Zurich, Switzerland

A 2-2 cascaded multi-standard ΔΣ modulator achieves a DR of 88/79/67dB in EDGE/UMTS/WLAN mode, respectively. With a high linearity of -92dB THD and 34dBm IIP3 for EDGE, this ADC is suitable for wireless applications. Implemented in 0.13µm CMOS and occupying 0.4mm², the modulator covers 0.1-to-10MHz signal bandwidth with scalable power consumption between 2.9 and 20.5mW from a 1.2V supply.

**13.3 A 1.2V 121-Mode CT ΔΣ Modulator for Wireless Receivers in 90nm CMOS** **9:30 AM**

*S. Ouzounov,* NXP Semiconductors, Eindhoven, The Netherlands

A reconfigurable CT 5th-order 1b ΔΣ modulator is presented. The DR/BW is programmable from 85dB@100kHz to 52dB@10MHz in 121 steps. Implemented in a 90nm CMOS process, the 0.36mm² IC includes 2 ΔΣ modulators, a bandgap reference, and a decimator. The power consumption of a single ADC in different modes ranges from 1.44 to 7mW at 1.2V supply.

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**13.4 A 5th-Order CT/DT Multi-Mode ΔΣ Modulator** **10:15 AM**

*B. Putter*, NXP Semiconductors, Zurich, Switzerland

A 5th-order CT/DT multi-mode ΔΣ ADC for the digitisation of baseband signals is presented. For accurate loop characteristics, the design uses DT switched-capacitor OTAs for the second- to fifth-stage integrators while the CT first-stage integrator provides anti-alias filtering. Implemented in 65nm CMOS, the design achieves 88/82/73dB DR for EDGE/CDMA/UMTS and draws <1.5mA from a 2.5V supply.

**13.5 A 65fJ/Conversion-Step 0-to-50MS/s 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS** **10:45 AM**

*J. Craninckx,* IMEC, Leuven, Belgium

A fully dynamic SAR ADC is proposed that uses passive charge-sharing and an asynchronous controller to achieve low power consumption. No active circuits are needed for high-speed operation and all static power is removed, offering a power consumption proportional to sampling frequency from 50MS/s down to 0. The prototype implementation in 90nm digital CMOS achieves 7.8 ENOB, 49dB SNDR at 20MS/s consuming 290µW. This results in a FOM of 65fJ/conversion-step.

**13.6 A 14b 40MS/s Redundant SAR ADC with 480MHz Clock in 0.13µm CMOS** **11:15 AM**

*M. Hesener,* Infineon Technologies, Neubiberg, Germany

A 2-channel time-interleaved 40MS/s SAR ADC with redundancy is presented. The 0.13µm 1.5V CMOS design runs at 480MHz iteration clock and features 89dB THD and 81dB SNDR. Including the PLL, the second-order anti-alias filter, and reference buffer, the chip consumes 66mW and occupies 0.55mm .

**13.7 A 1.5V 200MS/s 13b 25mW DAC with Randomized Nested Background Calibration in 0.13µm CMOS** **11:45 AM**

*M. Clara,* Infineon Technologies, Villach, Austria

Time-domain randomization of the unit current-cell refresh period converts the tonal behavior of cyclic background calibration into noise. Together with nested calibration of all DAC-segments a low-frequency SFDR of 83.7dB is achieved. The chip is fabricated in a standard 0.13µm CMOS process. Clocked at 200MHz, it consumes 25mW from a 1.5V supply.